WHAT IS CL AIMED IS:

1. A process of forming metal surfaces on a bare metal chip, the metal chip comprising at least one metal interconnect formed on a semiconductor substrate, at least a portion of the metal interconnect being exposed to the environment, the process comprising:

applying a metal on the exposed portion of the metal interconnect;

performing a maskless chemical process that converts a layer of the metal into a bondable layer compatible with a wire bonding; and

bonding a metal wire to the bondable layer.

2. The process of Claim 1, wherein the at least one metal interconnect is substantially copper.

3. The process of Claim 1, wherein the metal wire comprises aluminum or gold or metal alloy.

4. The process of Claim 1, wherein the bonding is performed by an ultrasonic wire bonding, a thermosonic wire bonding, a welding or combination thereof.

5. The process of Claim 1, wherein the semiconductor substrate is selected from the group consisting of: silicon, GaAs, and InP.

6. The process of Claim 1, wherein the process is additionally applied to any structure formed on the semiconductor substrate on which the wire bonding is carried out.

7. A process of forming metal surfaces on a bare metal chip, the metal chip comprising at least one metal interconnect formed on a semiconductor substrate, at least a portion of the metal interconnect being exposed to the environment, the process comprising:

applying a noble metal on the exposed portion of the metal interconnect;

performing a chemical process that causes a layer of the noble metal to convert into a bondable layer compatible with a wire bonding; and

bonding a metal wire to the bondable layer.

8. The process of Claim 7, wherein the chemical process causes atoms of the noble metal to be diffused and mixed with metal atoms of the metal interconnect.

9. The process of Claim 8, wherein the chemical process comprises one of the following: an immersion process, a dip process or an electroless process.

10. The process of Claim 7, wherein the noble metal substantially comprises Ag, Au, Pd, Pt, Ru, Rh, Re, Os, Ir or any alloy thereof.

11. The process of Claim 7, wherein the at least one metal interconnect is substantially copper.

12. The process of Claim 7, wherein the metal wire comprises aluminum or gold or metal alloy.

13. The process of Claim 7, wherein the bonding is performed by an ultrasonic wire bonding, a thermosonic wire bonding, a welding or combination thereof.

14. The process of Claim 7, wherein the semiconductor substrate is selected from the group consisting of: silicon, GaAs, and InP.

15. The process of Claim 7, wherein the process is additionally applied to any structure formed on the semiconductor substrate on which the wire bonding is carried out.

16. A process of forming metal surfaces on a bare metal chip, the metal chip comprising at least one metal interconnect formed on a semiconductor substrate, at least a portion of the metal interconnect being exposed to the environment, the process comprising:

depositing a layer of a noble metal on the exposed portion of the metal interconnect;

converting the layer of the noble metal to a bondable layer compatible with a wire bonding by a chemical process; and

bonding a metal wire to the bondable layer.

17. The process of Claim 16, wherein the chemical process comprises an immersion process, a dip silver process and an electroless process.

18. The process of Claim 16, wherein the at least one metal interconnect is substantially copper.

19. The process of Claim 16, wherein the metal wire comprises aluminum or gold.

20. The process of Claim 16, wherein the bonding is performed by an ultrasonic wire bonding, a thermosonic wire bonding, a welding or combination thereof.

21. The process of Claim 16, wherein the semiconductor substrate is selected from the group consisting of: silicon, GaAs, and InP.

22. The process of Claim 16, wherein the process is additionally applied to any structure formed on the semiconductor substrate on which the wire bonding is carried out.

23. A process of forming metal surfaces on a bare metal chip, the metal chip comprising at least one metal interconnect formed on a semiconductor substrate, at least a portion of the metal interconnect being exposed to the environment, the process comprising:

forming a layer of a low melting point metal whose melting temperature is relatively low on the exposed portion of the metal interconnect;

converting the layer of the low melting point metal into a bondable layer compatible with a wire bonding by a chemical process; and

bonding a metal wire to the bondable layer.

24. The process of Claim 23, wherein the chemical process comprises an electroless tin process, a dip tin process and an electroless bismuth process.

25. The process of Claim 23, wherein the at least one metal interconnect is substantially copper.

26. The process of Claim 23, wherein the metal wire comprises aluminum or gold.

27. The process of Claim 23, wherein the bonding is performed by an ultrasonic wire bonding, a thermosonic wire bonding, a welding or combination thereof..

28. The process of Claim 23, further comprising performing a chemical reaction, a heat treatment or combination thereof on the bondable layer in order to increase the adhesion of the bondable layer on the exposed portion of the metal interconnect.

29. The process of Claim 23, wherein the melting temperature is below 350°C.

30. The process of Claim 23, wherein the semiconductor substrate is selected from the group consisting of: silicon, GaAs, and InP.

31. The process of Claim 23, wherein the process is additionally applied to any structure formed on the semiconductor substrate on which the wire bonding is carried out.

32. A process of forming an electrical connection between a metal wire and at least one metal interconnect supported on a semiconductor substrate, the process comprising:

forming the at least one metal interconnect on the semiconductor substrate;

depositing a passivation layer on the metal interconnect, at least a portion of the metal interconnect being exposed to the environment through an opening formed on the passivation layer;

applying a low melting point metal whose melting temperature is relatively low on the exposed portion of the metal interconnect;

converting a layer of the low melting point metal into a bondable layer compatible with a wire bonding on the exposed portion of the metal interconnect; and

bonding a metal wire to the bondable layer.

33. The process of Claim 32, wherein the at least one metal interconnect is substantially copper.

34. The process of Claim 32, wherein the metal wire comprises aluminum or gold or metal alloy.

35. The process of Claim 32, wherein the bonding is performed by an ultrasonic wire bonding, a thermosonic wire bonding, a welding or combination thereof.

36. The process of Claim 32, further comprising performing a heat treatment on the bondable layer in order to increase the adhesion of the bondable layer on the exposed portion of the metal interconnect.

37. The process of Claim 32, wherein the semiconductor substrate is selected from the group consisting of: silicon, GaAs, and InP.

38. The process of Claim 32, wherein the process is additionally applied to any structure formed on the semiconductor substrate on which the wire bonding is carried out.

39. A process of forming metal surfaces on a bare metal chip, the metal chip comprising at least one metal interconnect formed on a semiconductor substrate, at least a portion of the metal interconnect being exposed to the environment, the process comprising:

forming a layer of solder particles of a low melting point metal whose temperature is relatively low on the exposed portion of the metal interconnect;

converting the layer of the solder particles into a bondable layer compatible with a wire bonding; and

bonding a metal wire to the bondable layer.

40. The process of Claim 39, wherein the at least one metal interconnect is substantially copper.

41. The process of Claim 39, wherein the metal wire comprises aluminum or gold.

42. The process of Claim 39, wherein the bonding is performed by an ultrasonic wire bonding, a thermosonic wire bonding, a welding or combination thereof.

43. The process of Claim 39, further comprising performing a chemical reaction, a heat treatment or combination thereof on the bondable layer in order to increase the adhesion of the bondable layer on the exposed portion of the metal interconnect.

44. The process of Claim 39, wherein the semiconductor substrate is selected from the group consisting of: silicon, GaAs, and InP.

45. The process of Claim 39, wherein the process is additionally applied to any structure formed on the semiconductor substrate on which the wire bonding is carried out.

46. The process of Claim 39, wherein the forming comprises:

providing a tacky layer on the exposed portion of the metal interconnect; and

applying the solder particles of the low melting point metal on the tacky layer, thus forming the layer of the solder particles.

47. A process of forming metal surfaces on a bare metal chip, the metal chip comprising at least one metal interconnect formed on a semiconductor substrate, at least a portion of the metal interconnect being exposed to the environment, the process comprising:

forming a layer of fine particles of a noble metal or an alloy thereof on the exposed portion of the metal interconnect;

converting the layer of the solder particles into a bondable layer compatible with a wire bonding on the exposed portion of the metal interconnect by performing a chemical reaction, a heat treatment or combination thereof on the layer of fine particles; and

bonding a metal wire to the bondable layer.

48. The process of Claim 47, wherein the at least one metal interconnect is substantially copper.

49. The process of Claim 47, wherein the metal wire comprises aluminum or gold.

50. The process of Claim 47, wherein the bonding is performed by an ultrasonic wire bonding, a thermosonic wire bonding, a welding or combination thereof.

51. The process of Claim 47, wherein the forming comprises:

providing a tacky layer on the exposed portion of the metal interconnect; and

applying the fine particles on the tacky layer, thus forming the layer of the fine particles.

52. The semiconductor integrated circuit of Claim 47, wherein the semiconductor substrate is selected from the group consisting of: silicon, GaAs, and InP.

53. A semiconductor integrated circuit, comprising:

a bare semiconductor chip comprising;

a semiconductor substrate; and

a metal interconnect formed on the semiconductor substrate, at least a portion of the metal interconnect being exposed to the environment;

a layer of a noble metal formed on the portion of the metal interconnect, and compatible with a wire bonding; and

a metal wire bonded to the layer of the noble metal.

54. The semiconductor integrated circuit of Claim 53, wherein the noble metal substantially comprises Ag, Au, Pd, Pt, Ru, Rh, Re, Os, Ir or any alloy thereof.

55. The semiconductor integrated circuit of Claim 53, wherein the metal interconnect comprises a copper.

56. The semiconductor integrated circuit of Claim 53, wherein the metal wire comprises an aluminum wire or a gold wire or metal alloy wire.

57. The semiconductor integrated circuit of Claim 53, wherein the semiconductor substrate is selected from the group consisting of: silicon, GaAs, and InP.

58. A semiconductor integrated circuit, comprising:

a bare semiconductor chip comprising;

a semiconductor substrate; and

a metal interconnect formed on the semiconductor substrate, at least a portion of the metal interconnect being exposed to the environment;

a layer of a low melting point metal formed on the exposed portion of the metal interconnect, and compatible with a wire bonding, a melting temperature of the low melting point metal being relatively low; and

a metal wire bonded to the layer of the low melting point metal.

59. The semiconductor integrated circuit of Claim 58, wherein the low melting metal comprises Sn, In, Bi, Pb and an alloy thereof.

60. The semiconductor integrated circuit of Claim 58, wherein the metal interconnect comprises a copper.

61. The semiconductor integrated circuit of Claim 58, wherein the metal wire comprises an aluminum wire or a gold wire.

62. The semiconductor integrated circuit of Claim 58, wherein the melting temperature is below 350°C.

63. The semiconductor integrated circuit of Claim 58, wherein the semiconductor substrate is selected from the group consisting of: silicon, GaAs, and InP.

64. A semiconductor integrated circuit, comprising:

a bare semiconductor chip comprising;

a semiconductor substrate; and

a metal interconnect formed on the semiconductor substrate, at least a portion of the metal interconnect being exposed to the environment;

a layer of solder particles of a low melting point metal formed on the exposed portion of the metal interconnect, and compatible with a wire bonding, a melting temperature of the low melting point metal being relatively low; and

a metal wire bonded to the layer of solder particles.

65. The semiconductor integrated circuit of Claim 64, wherein the low melting point metal comprises Sn, In, Bi, Pb and an alloy thereof.

66. The semiconductor integrated circuit of Claim 64, wherein the metal interconnect comprises a copper.

67 The semiconductor integrated circuit of Claim 64, wherein the metal wire comprises an aluminum wire or a gold wire.

68. The semiconductor integrated circuit of Claim 64, wherein the melting temperature is below 350°C.

69. The semiconductor integrated circuit of Claim 64, wherein the semiconductor substrate is selected from the group consisting of: silicon, GaAs, and InP.

70. A semiconductor integrated circuit, comprising:

a bare semiconductor chip comprising;

a semiconductor substrate; and

a metal interconnect formed on the semiconductor substrate, at least a portion of the metal interconnect being exposed to the environment;

a layer of particles of a noble metal or an alloy thereof formed on the exposed portion of the metal interconnect and compatible with a wire bonding; and

a metal wire bonded to the layer of solder particles.

71. The semiconductor device of Claim 70, wherein the noble metal substantially comprises Ag, Au, Pd, Pt, Ru, Rh, Re, Os or Ir.

72. The semiconductor integrated circuit of Claim 70, wherein the metal interconnect comprises a copper.

73. The semiconductor integrated circuit of Claim 70, wherein the metal wire comprises an aluminum wire or a gold wire.

74. The semiconductor integrated circuit of Claim 70, wherein the semiconductor substrate is selected from the group consisting of: silicon, GaAs, and InP.

75. A semiconductor integrated circuit, comprising:

a bare semiconductor chip comprising;

a semiconductor substrate; and

a metal interconnect formed on the semiconductor substrate, at least a portion of the metal interconnect being exposed to the environment;

a layer of a metal formed on the portion of the metal interconnect by a maskless chemical process, and compatible with a wire bonding; and

a metal wire bonded to the layer of the metal.

76. The semiconductor integrated circuit of Claim 75, wherein the metal interconnect comprises a copper.

77. The semiconductor integrated circuit of Claim 75, wherein the metal wire comprises an aluminum wire or a gold wire or metal alloy wire.

78. The semiconductor integrated circuit of Claim 75, wherein the semiconductor substrate is selected from the group consisting of: silicon, GaAs, and InP.